

Appln. No. 10/747,741
Reply to Office Action of August 8, 2007
Amendment dated: February 8, 2008

REMARKS

Applicants have canceled claims 9-11 and therefore the claim objections set forth by the Examiner for these claims are now rendered moot. In regard to the objection to claim 18, Applicants have modified claim 18 in accordance with the Examiner's suggestions. Accordingly, Applicants respectfully request that the Examiner withdraw the objection to claim 18.

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 U.S.C. sections 102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention. More specifically, by this amendment, Applicants have modified each of the remaining independent claims to specify that the reset switches for each pixel element is a depletion type transistor. In contrast with the present invention, the Miwada prior art reference is merely directed to a charge transfer device wherein the reset drain regions for resetting or draining charges in the floating diffusion region is connected via a capacitor to a constant potential terminal.

The absorption drain region incorporates a voltage booster that raises the amplitude of the transfer pulse to a level that is higher than the power source voltage. The output voltage of the voltage booster is applied to the absorption drain region. The channel potential beneath the barrier gate electrode is therefore set lower than that which is beneath the reset gate electrodes.

In accordance with the presently claimed invention, the reset switches are comprised of depletion type transistors. In contrast, the Miwada reference merely describes that the floating diffusion region 7 is connected to the gate electrode of an

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enhancement type n channel MOS transistor in source follower arrangement which is comprised of the transistor Tr1 and a depression type n channel MOS transistor Tr2. This is described specifically in column 4 at ll. 49-54.

Significantly, the reference does not disclose or even remotely suggest that the reset switches are comprised of a depletion type transistor. Accordingly, in light of the foregoing, Applicants submit that all claims now stand in condition for allowance.

Respectfully submitted,

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